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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,987	07/11/2005	Dolf Henricus Jozef Van Casteren	NL 030036	7997
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EXAMINER				
TRAN, THUY V				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/541,987

Applicant(s)

VAN CASTEREN ET AL.

Examiner

Thuy V. Tran

Art Unit

2821

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on amendment submitted on 01/08/2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9, 11 and 20-41 is/are allowed.
- 6) ☒ Claim(s) 1-8, 10 and 12-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 September 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-849)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

This Office Action is in response to the Applicants' amendment submitted on 01/08/2008. In virtue of this amendment, claims 1-41 remain pending in the instant application.

Response to Applicants' amendment

1. Applicants' amendments to claims 1, 7, and 12 submitted on 01/08/2008 necessitate new grounds of rejections. Therefore, claims 1, 7, and 12 and their dependents are now being rejected as follows:

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 7, the recitation "wherein the on-time ... resonant circuit" in lines 13-14 renders the claim indefinite as to what element/device the on-time belongs to. Clarification is required.

Claim 8 is also reject under 35 U.S.C. 112, second paragraph, as being dependent upon claim 7.

4. Claim 7 recites the limitation "the on-time" in line 13. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(c), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-8, 10, and 12-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (U.S. Patent No. 6,272,024 B2).

With respect to claims 1 and 19, Uchida discloses, in Figs. 1-3, a circuit for providing power to a load [14] with a predetermined specification comprising (1) a transformer [2] having a primary winding [8] and a secondary winding [9]; said secondary winding [9] being part of a resonant circuit [9, 11], (2) first and second connection nodes [12, 13] for coupling of the load [14] in series to the secondary winding [9], (3) a switch [3] coupled in series to the primary winding [8], an on-time and an off-time of the switch [3] being controllable by a control element [5], for generating a voltage pulse (see Fig. 2; col. 4, lines 15-16) over the primary winding [8], and (4) a diode [16] (see Fig. 1) coupled in series with a surge suppressor [17, 18] and both coupled in parallel to the primary winding [8] for absorbing the surges developed across the primary winding [8] of the transformer (see col. 4, lines 52-59) and for forward biased by the voltage developed in the primary winding [8] of the transformer [2] when the switch [3] is turned

off (see col. 4, lines 30-32) and thus resulting in demagnetizing the transformer during the off-time of the switch [3], the on-time and the off-time of the switch [3] being predetermined (which is at a rate required for holding the converter output voltage constant; see col. 4, lines 15-16).

Uchida does not disclose that (i) the load is a gaseous discharge lamp which comprises a high-intensity discharge lamp, (ii) the diode [16] is directly coupled in parallel to the primary winding [8] of the transformer [2] (which means that there is no such arrangement of the surge suppressor [17, 18]), and (iii) the on-time (of the switch [3]) is higher than half of an oscillation period of the resonant circuit [9, 11]. These differences, however, are not of patentable merits since (i) it is believed that the circuit of Fig. 1 disclosed by Uchida is capable of working properly without the surge suppressor [17, 18], or in other words, the surge suppressor [17, 18] and its function of absorbing the surges that develop across the transformer primary winding [8] can be omitted if not desired, (ii) the load can be a gaseous high-intensity discharge lamp load, which has been commonly operated by a flyback transformer (*see prior art of record to Daspit; U.S. Patent No. 4,441,053; see Fig. 7 and Abstract, lines 1-4*), and (iii) both resonant capacitor [11] and the load [14] are connected in parallel with the secondary winding [9] sharing the same potential thereof and a change of the load characteristics (e.g. different load lamp) and that of corresponding capacitance value of the resonant capacitor [11] for an adjustment of an oscillation period of the resonant circuit formed by the secondary winding [9] and the capacitor [11] would be obviously made upon a particular circumstance with the availability of type of lamp, type of resonant capacitor, etc.. Consequently, to implement the circuit arrangement of Uchida with a gaseous discharge lamp as the load with a corresponding capacitance value of the resonant capacitor so as to maintain the on-time of the switch at a level higher than half of the oscillation period of the

resonant circuit and to eliminate the surge suppressor [17, 18] and its function distributed to the transformer in the circuit of Uchida upon a desirability or expectation for achieving a particular end or result in a given circumstance would have been deemed obvious to a person skilled in the art of electronics.

With respect to claim 2, Uchida discloses, in Fig. 1, a capacitor [11] is added in parallel to the secondary winding [9] for adjusting the resonance period of the resonant circuit [9, 11].

With respect to claim 3, Uchida obviously discloses all of the claimed subject matter, as expressly recited in claim 1, except that the transformer has a couple factor smaller than 1. However, this difference is not of patentable merit since it has been commonly known in the art that the worse the coupling factor, the higher the necessary quality factor Q (*see Prior Art of Record to Jansen, U.S. Patent No. 5,608,613; col. 4, lines 66-67 and col. 5, lines 1-2*). Accordingly, to perform a coupling factor of smaller than 1 for the windings [8, 9] of the transformer of Uchida to improve the high quality factor Q of the circuit of Uchida would have been deemed obvious to a person skilled in the art.

With respect to claim 4, Uchida discloses that the control element [5] is selected to cause the on-time of the switch to be at least half of a resonance frequency of the resonance circuit (see col. 5, lines 17-32).

With respect to claim 5, Uchida discloses that the control element [5] is selected to cause the off-time of the switch to be sufficient to reduce a current in the diode [16] to substantially zero (at time from t_1 to t_2 ; see Fig. 3) during demagnetization of the transformer (see col. 5, lines 33-52).

With respect to claim 6, Uchida discloses that the circuit is characterized in that a resistor [18] is connected in series to the diode [16] (see Fig. 1) to reduce the off- time.

With respect to claim 7, as to the best interpretation, Uchida discloses, in Figs. 1-3, a circuit and a corresponding method for providing power to a load [14] comprising the steps of (1) applying a number of voltage pulses (see Fig. 2) to a primary winding [8] (see Fig. 1) of a transformer [2] so as to produce each time a high-voltage pulse (see Fig. 2) on a secondary winding [9] of the transformer, wherein said secondary winding is part of a resonant circuit and wherein the high voltage pulse is shaped by transformer inductances (of windings [8, 9]; see Fig. 1) and capacitances (of capacitor [11]; see Fig. 1) at a secondary side to create a load pulse, (2) applying the load pulse to the load [14], and (3) providing, between every application of a voltage pulse, a current path through a diode [16] coupled in series with a surge suppressor [17, 18] and both coupled in parallel to the primary winding [8] for absorbing the surges developed across the primary winding [8] of the transformer (see col. 4, lines 52-59) and for forward biased by the voltage developed in the primary winding [8] of the transformer [2] when the switch [3] is turned off (see col. 4, lines 30-32) and thus resulting in demagnetizing the transformer and preventing saturation of the transformer. Uchida does not disclose that (i) the load is a gaseous discharge lamp which comprises a high-intensity discharge lamp, (ii) the diode [16] is directly coupled in parallel to the primary winding [8] of the transformer [2] (which means that there is no such arrangement of the surge suppressor [17, 18]), and (iii) the on-time (of the switch [3]) is higher than half of an oscillation period of the resonant circuit [9, 11]. These differences, however, are not of patentable merits since (i) it is believed that the circuit of Fig. 1 disclosed by Uchida is capable of working properly without the surge suppressor [17, 18], or in other words,

the surge suppressor [17, 18] and its function of absorbing the surges that develop across the transformer primary winding [8] can be omitted if not desired, (ii) the load can be a gaseous high-intensity discharge lamp load, which has been commonly operated by a flyback transformer (*see prior art of record to Daspit; U.S. Patent No. 4,441,053; see Fig. 7 and Abstract, lines 1-4*), and (iii) both resonant capacitor [11] and the load [14] are connected in parallel with the secondary winding [9] sharing the same potential thereof and a change of the load characteristics (e.g. different load lamp) and that of corresponding capacitance value of the resonant capacitor [11] for an adjustment of an oscillation period of the resonant circuit formed by the secondary winding [9] and the capacitor [11] would be obviously made upon a particular circumstance with the availability of type of lamp, type of resonant capacitor, etc.. Consequently, to implement the circuit arrangement of Uchida with a gaseous discharge lamp as the load with a corresponding capacitance value of the resonant capacitor so as to maintain the on-time of the switch at a level higher than half of the oscillation period of the resonant circuit and to eliminate the surge suppressor [17, 18] and its function distributed to the transformer in the circuit of Uchida upon a desirability or expectation for achieving a particular end or result in a given circumstance would have been deemed obvious to a person skilled in the art of electronics.

With respect to claim 8, Uchida obviously discloses all of the claimed subject matter, as expressly recited in claim 7, except for an explicit teaching that a first series of pulses is applied to ignite the lamp, and a second series of pulses is applied to operate the lamp during the electrode heating phase of said lamp. This difference, however, is not of patentable merit since the circuit of Uchida including the switching circuit and the transformer is operable to perform such functions (see Figs. 2-3) and to hold the output voltage constant (see col. 4, lines 14-16).

For these advantages, to operate the lamp with the circuit of Uchida by applying a first series of pulses to ignite the lamp, and a second series of pulses to operate the lamp during the electrode heating phase of said lamp would have been deemed obvious to a person skilled in the art.

With respect to claim 10, Uchida discloses that the off-time of the switch is chosen to be higher than a time necessary to reduce a current through the diode [16] to substantially zero (at time from t_1 to t_2 ; see Fig. 3; col. 5, lines 33-52).

With respect to claim 12, Uchida discloses, in Figs. 1-3, a circuit for providing power to a load [14] comprising (1) a transformer [2] having a primary winding [8] and a secondary winding [9]; the load [14] being connected to the secondary winding [9] and the secondary winding being part of a resonant circuit [9, 11], (2) a switch [3] coupled to the primary winding [8], an on-time and an off-time of the switch [3] being controllable by a control element [5], for generating a voltage pulse (see Fig. 2; col. 4, lines 15-16) over the primary winding [8], and (3) a diode [16] (see Fig. 1) coupled in series with a surge suppressor [17, 18] and both coupled in parallel to the primary winding [8] for absorbing the surges developed across the primary winding [8] of the transformer (see col. 4, lines 52-59) and for forward biased by the voltage developed in the primary winding [8] of the transformer [2] when the switch [3] is turned off (see col. 4, lines 30-32) and thus resulting in demagnetizing the transformer during the off-time of the switch [3]. Uchida does not disclose that (i) the load is a gaseous discharge lamp which comprises a high-intensity discharge lamp, (ii) the diode [16] is directly coupled in parallel to the primary winding [8] of the transformer [2] (which means that there is no such arrangement of the surge suppressor [17, 18]), and (iii) the on-time (of the switch [3]) is higher than half of an oscillation period of the resonant circuit [9, 11]. These differences, however, are not of

patentable merits since (i) it is believed that the circuit of Fig. 1 disclosed by Uchida is capable of working properly without the surge suppressor [17, 18], or in other words, the surge suppressor [17, 18] and its function of absorbing the surges that develop across the transformer primary winding [8] can be omitted if not desired, (ii) the load can be a gaseous high-intensity discharge lamp load, which has been commonly operated by a flyback transformer (*see prior art of record to Daspit; U.S. Patent No. 4,441,053; see Fig. 7 and Abstract, lines 1-4*), and (iii) both resonant capacitor [11] and the load [14] are connected in parallel with the secondary winding [9] sharing the same potential thereof and a change of the load characteristics (e.g. different load lamp) and that of corresponding capacitance value of the resonant capacitor [11] for an adjustment of an oscillation period of the resonant circuit formed by the secondary winding [9] and the capacitor [11] would be obviously made upon a particular circumstance with the availability of type of lamp, type of resonant capacitor, etc.. Consequently, to implement the circuit arrangement of Uchida with a gaseous discharge lamp as the load with a corresponding capacitance value of the resonant capacitor so as to maintain the on-time of the switch at a level higher than half of the oscillation period of the resonant circuit and to eliminate the surge suppressor [17, 18] and its function distributed to the transformer in the circuit of Uchida upon a desirability or expectation for achieving a particular end or result in a given circumstance would have been deemed obvious to a person skilled in the art of electronics.

With respect to claim 13, Uchida discloses, in Fig. 1, that the circuit further comprises a capacitor [11] which is connected in parallel to the secondary winding [9] for adjusting the resonance period of a resonant circuit [9, 11] associated with the secondary winding [9].

With respect to claim 14, Uchida obviously discloses all of the claimed subject matter, as expressly recited in claim 12, except that the transformer has a couple factor smaller than 1. However, this difference is not of patentable merit since it has been commonly known in the art that the worse the coupling factor, the higher the necessary quality factor Q (*see Prior Art of Record to Jansen, U.S. Patent No. 5,608,613; col. 4, lines 66-67 and col. 5, lines 1-2*). Accordingly, to perform a coupling factor of smaller than 1 for the windings [8, 9] of the transformer of Uchida to improve the high quality factor Q of the circuit of Uchida would have been deemed obvious to a person skilled in the art.

With respect to claim 15, Uchida discloses that the control element [5] is selected to cause the on-time of the switch to be at least half of a resonance frequency of the resonance circuit (see col. 5, lines 17-32) associated with the secondary winding [9].

With respect to claim 16, Uchida discloses that the control element [5] is selected to cause the off-time of the switch to be sufficient to reduce a current in the diode [16] to substantially zero (at time from t_1 to t_2 ; see Fig. 3) during demagnetization of the transformer (see col. 5, lines 33-52).

With respect to claim 17, Uchida discloses that the circuit is characterized in that a resistor [18] is connected in series to the diode [16] (see Fig. 1) to reduce the off- time.

With respect to claim 18, Uchida discloses that the control element [5] is configured to control the switch to provide a voltage pulse to the primary winding [8] only if a free-running current through the diode [I_d] is substantially zero (see Figs. 2 and 3).

Allowable Subject Matter

7. Claims 9, 11, and 20-41 remain allowed.

Reasons for allowance of these claims were provided in the Office Action mailed on 10/17/2007.

Remarks and conclusion

8. The new abstract submitted on 01/08/2008 is accepted.
9. Applicants are noted that the statement “independent claims 1, 7, and 12 have been amended to include certain features of allowed claim 9 which are believed to render these claims patentable” made by Applicants at pages 18-19 is not true. The features recited therein are clearly disparate from each other. Specifically, for example, the limitation of “wherein the on-time is higher than half of an oscillation period of the resonant circuit” recited in claim 1 is not as the same as that of “a controller configured to ...choose the on-time of the switch to be higher than half of said maximum oscillation period” recited claim 9.

For the aforementioned,

- Claims 1-8, 10, and 12-19 remain rejected as being unpatentable over the teaching of Uchida (see details above); and
 - Claims 9, 11, and 20-41 are allowed.
10. Applicants’ amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuy V. Tran whose telephone number is (571) 272-1828. The examiner can normally be reached on M-F (8:00 AM -4:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Owens W. Douglas can be reached on (571) 272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

